

Application Note: Recommendations for Best Performance

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1 Introduction

The SX1261 and SX1262 are sub-GHz radio transceivers targeting for long range wireless applications, supporting both LoRa® modulation and GFSK modulation. They are capable to output a significantly large radio frequency (RF) signal in a 4 mm x 4 mm QFN24 package: the SX1261 can transmit up to +15 dBm and the SX1262 can transmit up to +22 dBm.

The transmission at such a high RF power generates significant heat which may transfer to the crystal resonator through the PCB. For long packet durations, this generates a frequency drift which may induce receive errors if no precautions are taken during PCB design.

This application note will explain how to set the optimal settings configuration (output power, SF/BW/payload size) and provides recommendations on PCB design to attain the best performance.

2 SX1261/2 Power Dissipation

2.1 SX1261/2 Power Considerations

The SX1261 is capable of delivering a +15 dBm maximum output power with a DC-DC converter or an LDO supply, from 1.8 V to 3.7 V.

The SX1262 is capable of delivering up to +22 dBm under the battery supply, from 1.8 V to 3.7 V.

Due to the power amplifier (PA) efficiency, a portion of this power is transformed in a RF signal, whereas the remaining part is sequentially

- dissipated into the SX1261/2 die
- propagated to the QFN24 package
- and finally transferred to the PCB.

Example with the SX1262:

At $P_{out} = 22$ dBm, which is equivalent to 158 mW, the typical total current consumption is 118 mA.

At 3.3 V, the total power consumption is given by the following calculation:

$$3.3 * 118 = 389 \text{ mW}$$

Out of this current, 158 mW are emitted on the transmission (TX) path of the RF signal.

Therefore $389 - 158 = 231$ mW are dissipated in the SX1262.

The figures below show the power consumption and heat dissipation, for the SX1261 and SX1262 at maximum output power (respectively +15 dBm and +22 dBm) at 25°C in both LDO and DC-DC configurations for different supply voltage conditions:

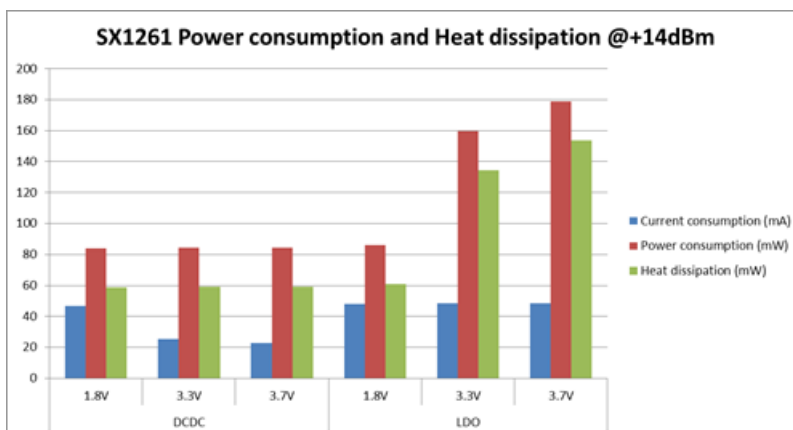


Figure 1: SX1261 Power Consumption & Heat Dissipation vs Supply Voltage & Power Mode

This figure shows the benefit of using the SX1261 DC-DC converter, as it allows to divide the power consumption by half compared to the LDO configuration. Moreover, the heat dissipation is maintained at a constant level with the supply voltage.

If an LDO configuration is chosen, the supply voltage should be kept as low as possible to minimize the power consumption and therefore the heat dissipation.

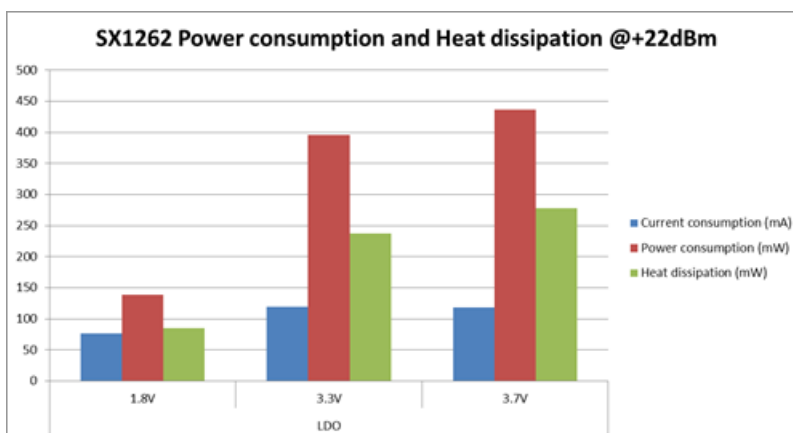


Figure 2: SX1262 Power Consumption & Heat Dissipation vs Supply Voltage & Power Mode

As the SX1262 PA has been optimized for a +22 dBm operation, less energy is dissipated during operation at +22 dBm power than at a lower output power setting, for example at +14 dBm. Reducing the output power will then reduce the power consumption but won't produce any positive impact in reducing the heat dissipation.

2.2 SX1261/2 Thermal Considerations

During a transmission, the heat generated in the SX1261/2 is transferred to the PCB. For a long transmission, this ends up in heating the crystal oscillator itself, making its frequency shift, and therefore will make the SX1261/2 RF frequency deviate. This frequency deviation should be minimized in order to ensure an optimum packet reception by the receiving device.

Depending on the application PCB constraints (number of layers, PCB dimensions, position of the crystal oscillator), there is a trade-off between Spreading Factor (SF), Bandwidth (BW), number of payload bytes for a given output power in order to limit this frequency deviation and therefore optimize the RF communication.

3 LoRa® and LoRaWAN™ Packet Duration

3.1 LoRa® Packet Structure:

The LoRa® packet is structured as follows:

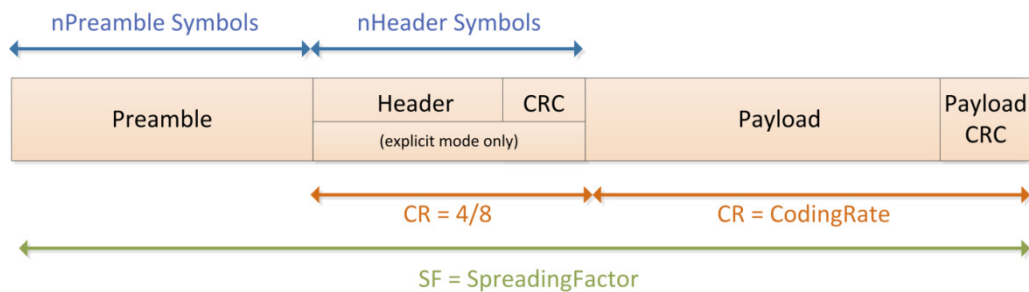


Figure 3: LoRa® Packet Format

The LoRa® packet durations are described in the SX1261/2 datasheet, and can also be calculated with the LoRa® Calculator. Both document and tool can be found on www.semtech.com.

SF, BW and number of payload bytes for the LoRaWAN™ applications are defined by the LoRaWAN™ regional parameters specification. The LoRaWAN™ packets duration is detailed in the following section.

3.2 LoRaWAN™ Packet Duration

In the LoRaWAN™ specification, the Payload field, called PHYPayload, consists of 3 fields:

- MAC Header (1Byte)
- MAC Payload (M Bytes), maximum length is region-specific and is specified in table 1 below.
- MIC (4Bytes)

The maximum payload length and following the maximum packet duration are summarized in table 1 for the lowest data rates (DR) of the LoRaWAN™ applications.

As per the SX1261/2 datasheet, it is advised to use the low data rate optimization (LDRO) feature when the symbol time exceeds 16.38 ms, which corresponds to the data rates with SF11 and SF12. For these configurations, the LDRO ensures an optimized packet reception, even if the long packet duration might provoke a carrier frequency deviation due to the PCB heating mechanism described in *section 2.2*.

Note:

- SF12 and SF11 configurations are highlighted in blue.
- The longest packet duration for the other SF are highlighted in green.
- Bandwidth expressed is 125 kHz.

Observations:

Table 1 shows us that the longest LoRaWAN™ packet without LDRO lasts:

- In the US 902 - 928 MHz band:
 - 400 ms for SF8 / BW 125 kHz with a maximum MAC payload length of 133 Bytes
 - 371 ms for SF10 / BW 125 kHz with a maximum MAC payload length of 19 Bytes
- In the other bands:
 - 698 ms for SF10 / BW 125 kHz with a maximum MAC payload length of 59 Bytes

Consequently for an SX1262 operating at +22 dBm in the US 902 – 928 MHz band, the frequency drift should be minimized for a maximum duration of 400 ms.

Furthermore for an SX1261 operating at +15 dBm and an SX1262 operating at +22 dBm in any of the regional bands, the frequency drift should be minimized for a maximum duration of 700 ms.

The maximum acceptable frequency drift $Freq_{drift-max}$ can be calculated from the SX1261/2 datasheet.

Table 1: LoRaWAN™ Packet Durations

Region	Band	DR	SF	Maximum MACPayload Length [Bytes]	Maximum PHYPayload Length [Bytes]	Symbol Time [ms]	Pmax	Device	Maximum Packet Duration [ms]
Europe	EU_863-870	0	12	59	64	32.768	15dBm	SX1261	2793.5
		1	11	59	64	16.384			1560.6
		2	10	59	64	8.192			698.4
		3	9	123	128	4.096			676.9
USA, Canada	US_902-928	0	10	19	24	8.192	22dBm	SX1262	370.7
		1	9	61	66	4.096			390.1
		2	8	133	138	2.048			399.9
		3	7	250	255	1.024			399.6
China	CN_779-787	0	12	59	64	32.768	15dBm	SX1261	2793.5
		1	11	59	64	16.384			1560.6
		2	10	59	64	8.192			698.4
		3	9	123	128	4.096			676.9
Australia	AU_915-928	0	12	59	64	32.768	22dBm	SX1262	2793.5
		1	11	59	64	16.384			1560.6
		2	10	59	64	8.192			698.4
		3	9	123	128	4.096			676.9
China	CN_470-510	0	12	59	64	32.768	22dBm	SX1262	2793.5
		1	11	59	64	16.384			1560.6
		2	10	59	64	8.192			698.4
		3	9	123	128	4.096			676.9
Asia	AS_923	0	12	59	64	32.768	15dBm	SX1261	2793.5
		1	11	59	64	16.384			1560.6
		2	10	59	64	8.192			698.4
		3	9	123	128	4.096			676.9
South Korea	KR_920-923	0	12	59	64	32.768	15dBm	SX1261	2793.5
		1	11	59	64	16.384			1560.6
		2	10	59	64	8.192			698.4
		3	9	123	128	4.096			676.9
India	IN_865-867	0	12	59	64	32.768	22dBm	SX1262	2793.5
		1	11	59	64	16.384			1560.6
		2	10	59	64	8.192			698.4
		3	9	123	128	4.096			676.9

4 SX1261/2 Measurements

The SX1261/2 frequency drift has been measured on both the SX1261 and SX1262, based on the Semtech reference design PCBs at 915 MHz.

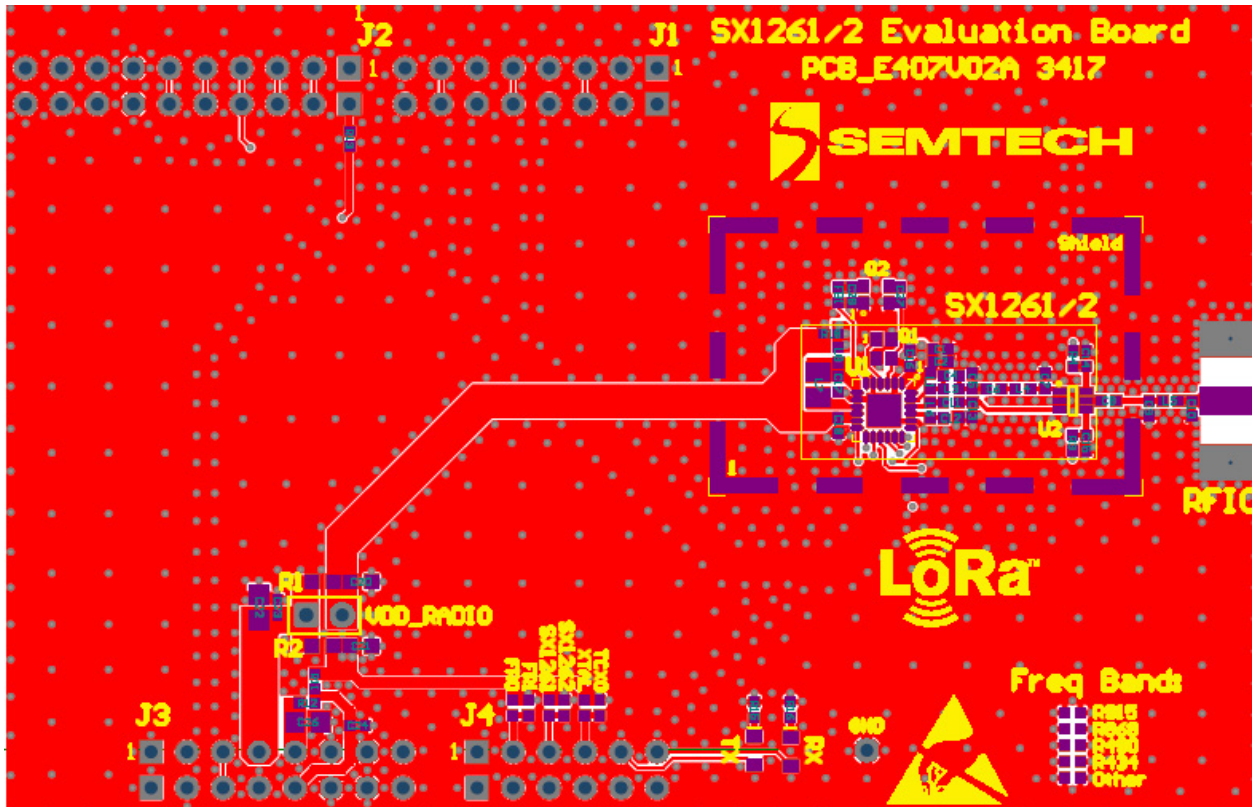


Figure 4: SX1261/2 Evaluation Board

Unless specified, the crystal oscillator used is an NDK NX2016SA (EXS00A-CS06465).

For the TCXO measurements, the TCXO used is an NDK NT2016SA.

The first section of this chapter studies the influence of temperature on the crystal behavior.

In the following sections, the frequency drift over time has been measured on SX1261 and SX1262 in different voltage conditions and different PCB configurations.

4.1 Crystal Oscillator Behavior versus Temperature

A typical temperature response of a crystal oscillator can be found in the following plot.

The typical behavior, depicted in black, is taken as reference.

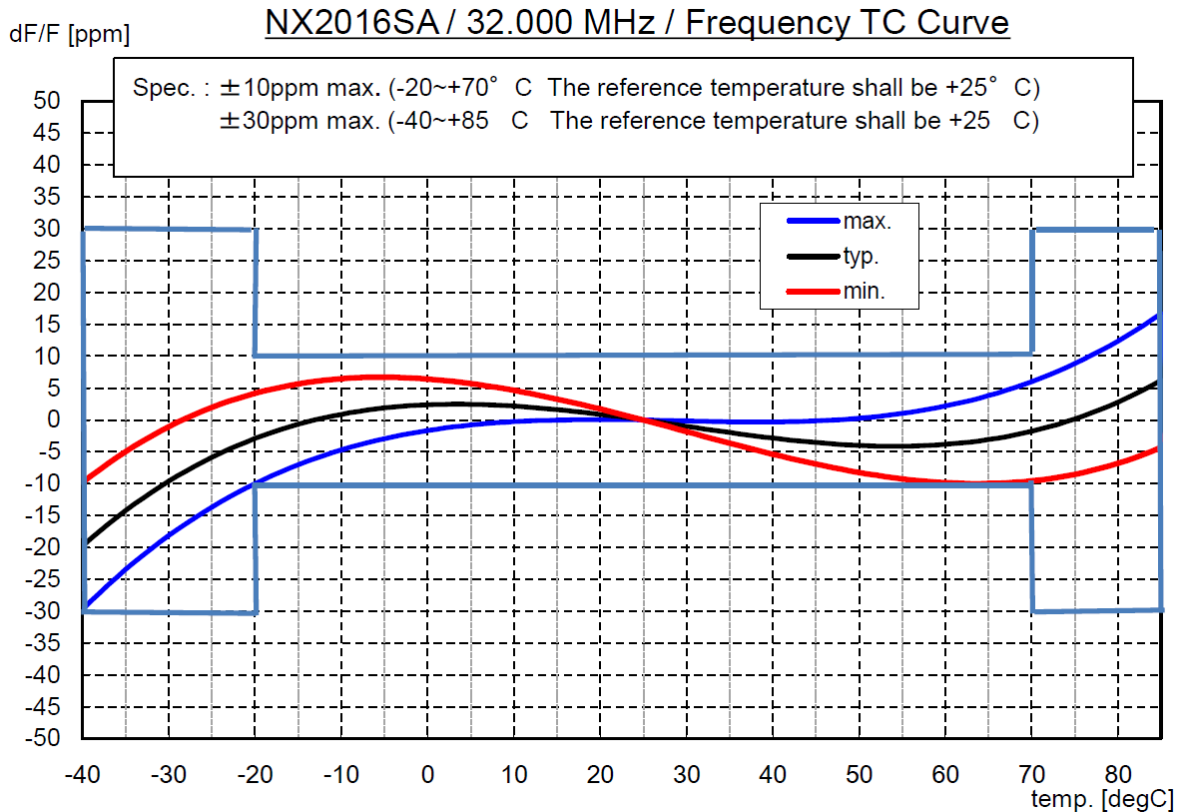


Figure 5: Crystal Oscillator Temperature Response

Observations:

- At 25 °C, the crystal frequency drops when the temperature increases. As a consequence the SX1261/2 RF carrier frequency will drop during a long RF transmission, as the heat generated by the SX1261/2 is transferred to the PCB, and then to the crystal oscillator.
- Around 0 °C and 55 °C, the crystal frequency response is flat against the temperature variation. In this case the SX1261/2 frequency drift is minimized at these temperatures. In the following sections, the frequency drift over time has been measured on SX1261 and SX1262 in different voltage conditions at 25 °C, where the crystal oscillator frequency drift with temperature is the highest, corresponding to the condition where the frequency drift is highest.
- At extreme temperatures (below -20 °C and above 70 °C), the crystal oscillator frequency drift is even higher. Care must be taken for applications working at those temperature conditions: depending on the application scenario (PCB size, output power, supply voltage, packet duration), a TCXO might be needed.

4.2 SX1261: Influence of Power Mode and Supply Voltage

The frequency drift of the SX1261 has been measured during a period of 2 seconds on the Semtech reference design PCB at 915 MHz, at 25 °C in a +15 dBm transmit operation, under 3 different supply voltages (1.8 V, 3.3 V and 3.7 V) in both DC-DC and LDO configurations.

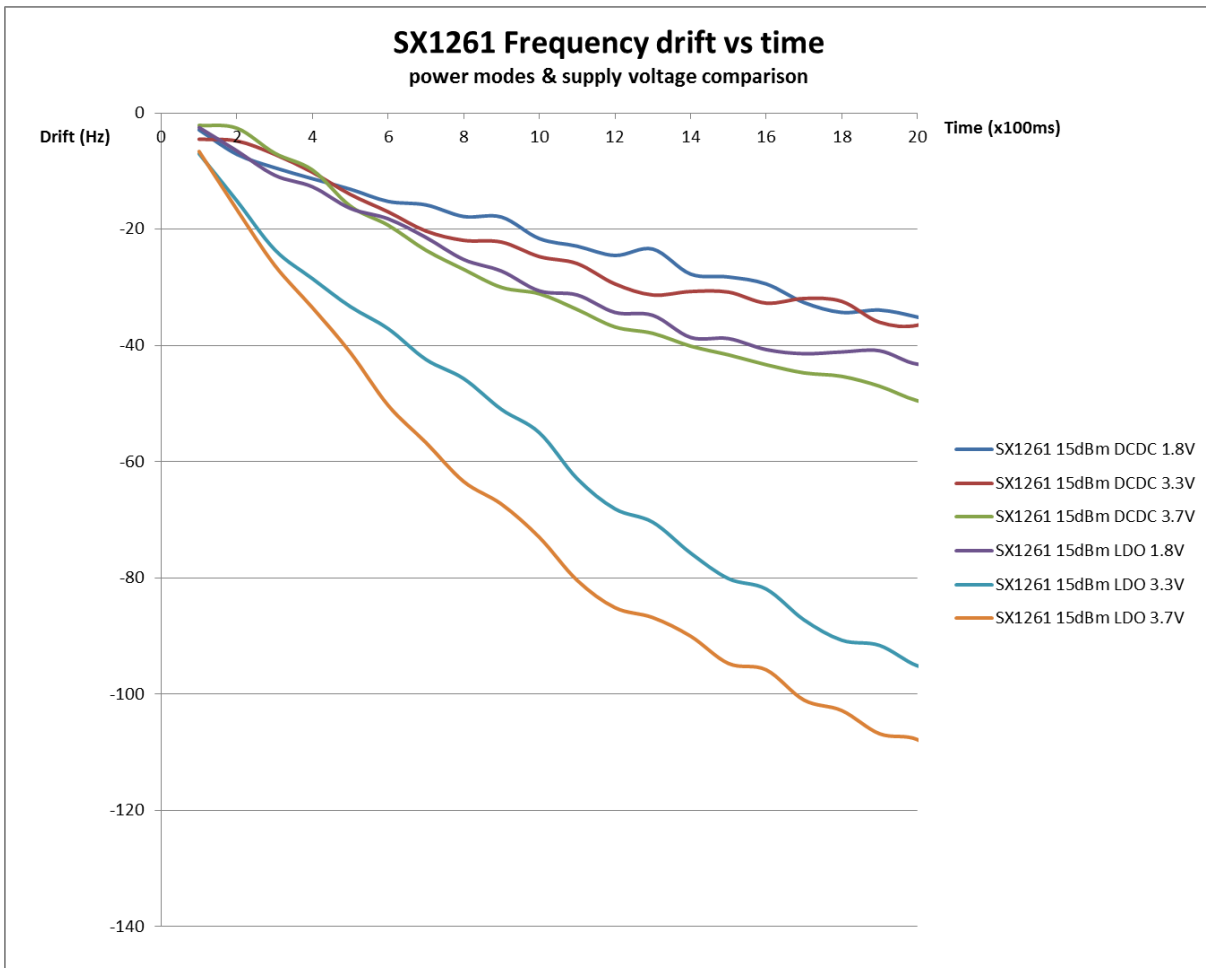


Figure 6: Frequency Drift vs Time for SX1261

Observations:

- As shown in *section 2.1*, the LDO configuration at 3.7 V is the mode where the power consumption and the heat dissipation are the highest. Consequently the frequency drift with time will be the highest in this power configuration.
- On the other hand, the frequency drift is minimized in DC-DC configuration, whatever the supply voltage.

4.3 PCB Solutions to Reduce Frequency Drift

A careful PCB design allows reducing the heat transfer between the SX1261/2 and the crystal oscillator, as shown below:

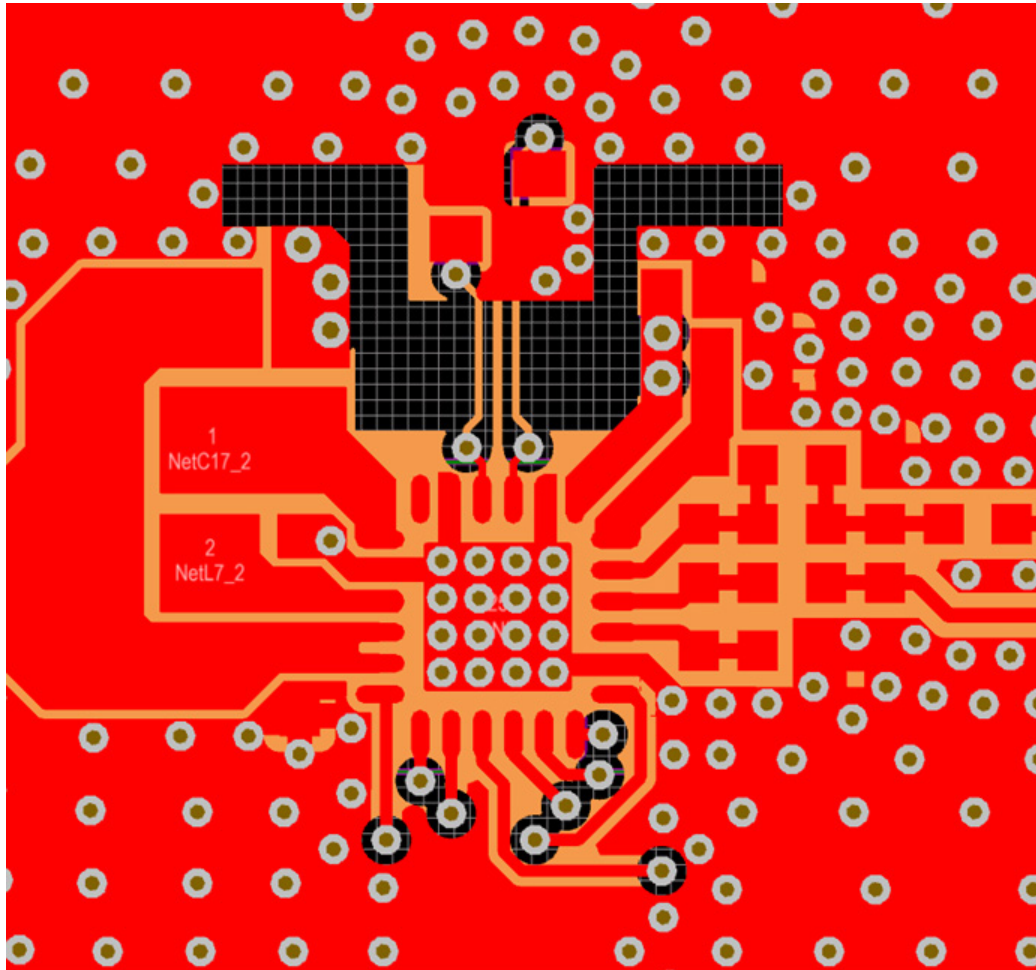


Figure 7: SX1261/2 PCB Adaptation with Thermal Insulation

Cuts in the top layer allow delaying the heat propagation from the SX1261/2 to the crystal oscillator. This adaptation acts as heat insulation to the crystal oscillator.

4.3.1 SX1261: Comparison between PCB Structures

3 different SX1261 PCB structures have been compared:

- 4-layer PCB similar to the PCB presented in *Figure 4: SX1261/2 Evaluation Board*
- 2-layer PCB
- PCB with thermal insulation around the crystal

The frequency drift has been measured on all 3 PCB structures, in the LDO 3.7 V configuration at 915 MHz, at 25 °C in a +15 dBm transmit operation. The reference plot of the SX1261 with thermal insulation in DC-DC mode at 3.3 V is also presented for comparison.

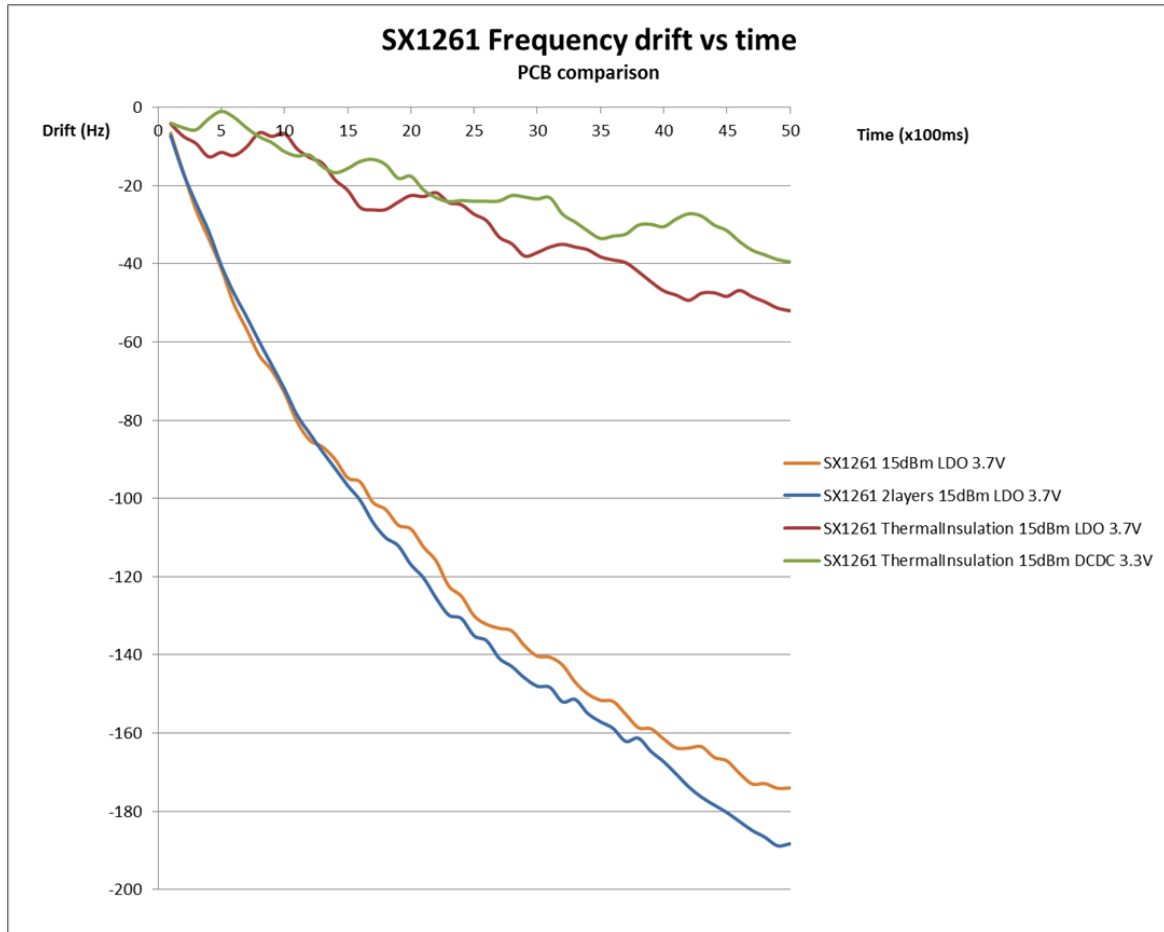


Figure 8: Frequency Drift vs Time for Different SX1261 PCB Structures

Observations:

- The 2-layers and 4-layers PCB both have the same drift rate. In the case of a standard PCB design, the number of layers has a minimum impact, as the heat transfer between the SX1261/2 occurs mainly on the top layer.
- Contrarily, the thermal insulation implemented in the SX1261 PCB allows minimizing the drift.

4.3.2 SX1262: Comparison between PCB Structures

3 different SX1262 PCB structures have been compared:

- 4-layer PCB similar to the PCB presented in *Figure 4: SX1261/2 Evaluation Board*
- same 4-layer PCB with a TCXO
- 4-layer PCB with thermal insulation around the crystal

The frequency drift has been measured during a 2 seconds period at 915 MHz, at 25°C in a +22 dBm transmit operation. The 3.7 V configuration, corresponding to the highest heat dissipation by the SX1262, has been retained.

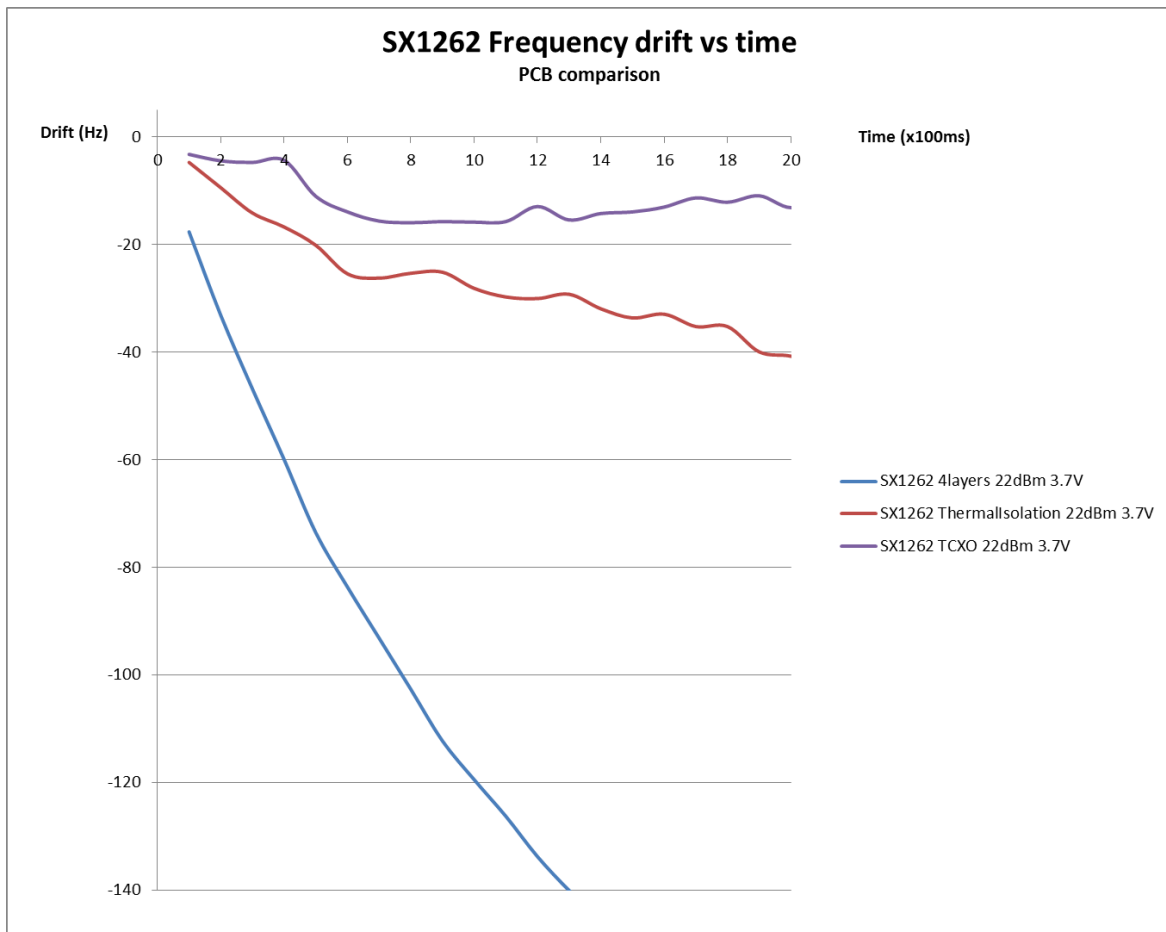


Figure 9: Frequency Drift vs Time for Different SX1262 PCB Structures

Observations:

- Without thermal insulation, the SX1262 frequency rapidly drifts beyond $Freq_{drift-max}$. Therefore either thermal insulation or a TCXO are necessary for a +22 dBm / 3.7 V operation.
- In the case of the PCB structure with thermal insulation, the frequency drift stays at $Freq_{drift-max}$ for a 400 to 500 ms transmit operation, but becomes marginal for a 1 second transmission. Consequently, for a 1 second transmission, a TCXO is necessary.

5 Conclusion

5.1 Recommendation for Operation of SX1261

For the SX1261, it is recommended to use the DC-DC configuration to reduce the power consumption the possibility of TX frequency drift during a packet transmission.

In the case of a LoRaWAN™ transmission, a standard PCB design allows us to keep the frequency drift below the maximum limit. In the case of other operations (LDO mode or non-LoRaWAN™), it is recommended to provide thermal insulation around the crystal during PCB design.

At extreme temperatures (below -20 °C and above 70 °C), it is recommended to use a TCXO.

5.2 Recommendation for Operation of SX1262

In the case of an SX1262 operating at +22 dBm in the US 902 – 928 MHz band, the frequency drift measured during the maximum LoRAWAN™ packet duration stays below the maximum limit, provided thermal insulation is implemented around the crystal during PCB design.

At extreme temperatures (below -20 °C and above 70 °C), it is recommended to use a TCXO.

For any other frequency bands corresponding to longer RF packet transmissions at +22 dBm, it is recommended to use a TCXO.

6 Revision History

Version	Date	Modifications
1.0	October 2017	First Release
1.1	January 2018	Correction of a typographical error in Table 1

7 Glossary

BW	BandWidth
CR	Coding Rate
CRC	Cyclical Redundancy Check
DR	Data Rate
GFSK	Gaussian Frequency Shift Keying
LDO	Low-Dropout
LDRO	Low Data Rate Optimization
LoRa®	LOng RANge modulation technique
LoRaWAN™	LoRa® low power Wide Area Network protocol
PA	Power Amplifier
PCB	Printed Circuit Board
PHY	Physical Layer
QFN	Quad Flat No-Lead
RF	Radio Frequency
SF	Spreading Factor
TCXO	Temperature-Compensated Crystal Oscillator



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Contact Information

Semtech Corporation
Wireless & Sensing Products
200 Flynn Road, Camarillo, CA 93012
E-mail: sales@semtech.com
Phone: (805) 498-2111, Fax: (805) 498-3804
www.semtech.com